OIPE
DEC 23 2004
PATENT & TRADEMARK OFFICE

10/670,510

OK to enter
LHN
02/15/05

SYNCHRONIZATION CIRCUIT

FILED OF THE INVENTION

The present invention relates to a synchronization circuit for synchronizing an asynchronously inputted signal with a clock, in a digital signal transmission apparatus.

BACKGROUND OF THE INVENTION

A conventional synchronization circuit synchronizes an asynchronously inputted signal with a synchronization clock, and outputs the synchronized signal (refer to Japanese Published Patent Application No. 5-327676 and USP4965814). Hereinafter, the conventional synchronization circuit will be described with reference to figure 17.

Figure 17 is a block diagram illustrating the construction of the conventional synchronization circuit.

With reference to figure 17, a flip-flop 1 receives an input signal SIN that is asynchronous to a synchronization clock SCK and an inverse clock nSCK that is output from an inverter 5, and the flip-flop 1 latches the input signal SIN at a timing of a rising edge of the inverse clock nSCK. A flip-flop 2 receives the input signal SIN and the synchronization clock SCK, and latches the input signal SIN at a timing of a rising edge of the synchronization clock SCK. A flip-flop 3 receives a signal that is selected by a selection circuit 4 and the synchronization clock SCK, and outputs a synchronizing signal SOUT at a timing of the rising edge of the synchronization clock SCK. The selection circuit 4 selects either the output of the